UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,447	10/26/2004	Hiroshi Takahara	260903US2PCT	4248

22850 7590 09/29/2008

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
CHOWDHURY, AFROZA Y	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
09/29/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/511,447	TAKAHARA ET AL.	
	Examiner	Art Unit	
	AFROZA Y. CHOWDHURY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8 and 10-21* is/are pending in the application.

4a) Of the above claim(s) *8 and 11-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,10 and 15-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/19/2008,7/8/2008,5/16/2008,2/11/2008,1/25/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Foreign references in IDS without English translation are not considered.

Response to Amendment

2. Applicant's amendment filed on **July 10, 2008** has been entered. Claims 1, 2, 4-8, and 10-21 are currently pending. As per last office action, claims 8 and 11-14 are withdrawn from further consideration as being drawn to nonelected groups.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "**each of the second switching elements has a plurality of transistor elements**" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1, 2, 4-8, and 10-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 1 and 2, "**an image signal applied to each pixel is executed only once during the one frame period**" is not described in the specification as originally filed.

Regarding claim 5, "**each of the second switching elements has a plurality of transistor elements**" is not described in the specification as originally submitted.

Regarding claims 16 and 17, there is no support for "**P-channel resistors**" in the specification as originally submitted.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 16 and 17, "**drive transistors are P-channel resistors**" is not clear. Is it a typo error for "P-channel transistors"?

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 5-7, 10, 15, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamazaki et al.** (US Patent 6,765,549) in view of **Kamezaki et al.** (US Patent 7,133,013).

As to claim 5, Yamazaki et al. teaches an EL display panel, comprising:

a source driver circuit (fig. 1(102)) which outputs an image signal (col. 8, lines 44-50);

EL elements (fig. 3(111)) arranged in a matrix (fig. 2(101, 104));

driver transistors (fig. 3(109)) which supply current to be passed through the EL elements (fig. 3(111));

first switching elements (fig. 3(105)) placed in current paths of the EL elements (fig. 3(111));

a first gate driver circuit (fig. 1(103)) which turns on and off the first switching elements (fig. 1(103)) for control (col. 8, line 67 – col. 9, line 9); and

a second gate driver circuit which turns on and off the second switching elements for control (col. 7, line 64); wherein:

the first gate driver circuit (fig. 1(103)) controls the first switching elements in an sate of off during one frame period (fig. 5, col. 10, lines 25-33).

Yamazaki et al. does not specifically teach second switching elements that constitute paths used to transmit the image signal to the driver transistors, each of the second switching elements has a plurality of transistor elements, each of the first switching elements and the each of the second switching elements are constituted so

that the first and second switching elements are controlled independently of each other for turning on and off by the first and second gate driver circuits.

However, it is obvious for an EL display to have second switching elements which constitute paths used to transmit the image signal to the driver transistors when a second gate driver is used and each of the first switching elements and the each of the second switching elements are constituted so that the first and second switching elements are controlled independently of each other for turning on and off by the first and second gate driver circuits.

Yamazaki et al. does not explicitly teach generating a plurality of stripe non-display areas on a display screen and moving the plurality of stripe non-display areas in a scanning direction of the gate driver circuit.

Kamezaki et al. teaches generating a plurality of stripe non-display areas (fig. 2(1a)) on a display screen and moving the plurality of stripe non-display areas in a scanning direction of the gate driver circuit (col. 4, lines 42-49, col. 7, lines 8-20).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to modify the drive method for an EL display of Yamazaki et al. using the idea of Kamezaki et al. of generating and moving a plurality of stripe non-display areas on a display screen in a scanning direction in order to achieve low power consumption and prevent flicker on a screen.

As to claim 6, Yamazaki et al. teaches an EL display panel where the first and second gate driver circuits are formed in a same process as the driver transistors and the source driver circuit is made of a semiconductor chip (col. 8, lines 44-50).

As to claim 7, Yamazaki et al. discloses an EL display panel wherein the second gate driver circuit selects a plurality of gate signal lines and supplies the image signal to the driver transistors of a plurality of pixel rows (col. 7, lines 60-64, col. 10, line 57 – col. 11, line 15).

As to claim 10, Yamazaki et al. teaches an EL display panel wherein the gate driver circuit is constructed of p-channel transistors (col. 16, lines 6-8, lines 32-42).

As to claim 15, Yamazaki et al. teaches an EL display apparatus comprising: the EL display panel and a receiver (fig. 17).

As to claim 20, Yamazaki et al. teaches an EL display panel wherein the driver transistors are P-channel transistors (col. 16, lines 6-9).

As to claim 21 Yamazaki et al. teaches an EL display panel wherein the first gate driver circuit is formed with P-channel transistors (col. 16, lines 6-9).

10. Claims 1-2, 4, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamazaki et al.** (US Patent 6,765,549) in view of **Sekiya et al.** (US Patent 6,583,775) and in further view of **Kamezaki et al.** (US Patent 7,133,013)..

As to claim 1, Yamazaki et al. discloses a drive method for an EL display panel, the EL display panel comprising:

EL elements (fig. 3(111)) arranged in a matrix (fig. 2(101, 104));

driver transistors (fig. 3(109)) which supply current to be passed through the EL elements (fig. 3(111));

first switching elements (fig. 3(105)) placed in current paths of the EL elements (fig. 3(111)); and

a gate driver circuit (fig. 1(103)) which turns on and off the first switching elements (fig. 3(105)) for control (col. 8, line 67 – col. 9, line 9);

wherein the gate driver circuit (fig. 1(103)) turns on and off the first switching elements two or more times during one frame period (fig. 5, col. 10, lines 25-33).

Yamazaki et al. does not explicitly teach an EL display panel where an operation for retaining an image signal applied to each pixel is retained only once during the one frame period.

Sekiya et al. teaches an EL display panel where an operation for retaining an image signal applied to each pixel is executed only once during the one frame period (col. 16, line 66 – col. 17, line 28).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to combine the image display panel apparatus of Sekiya et al. with the EL display device of Yamazaki et al. to make an EL display panel with improved picture quality.

Yamazaki et al. (as modified by Sekiya et al.) does not explicitly teach generating a plurality of stripe non-display areas on a display screen and moving the plurality of stripe non-display areas in a scanning direction of the gate driver circuit.

Kamezaki et al. teaches generating a plurality of stripe non-display areas (fig. 2(1a)) on a display screen and moving the plurality of stripe non-display areas in a scanning direction of the gate driver circuit (col. 4, lines 42-49, col. 7, lines 8-20).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to modify the drive method for an EL display of Yamazaki et al. (as modified by Sekiya et al.) using the idea of Kamezaki et al. of generating and moving a plurality of stripe non-display areas on a display screen in a scanning direction in order to achieve low power consumption and prevent flicker on a screen.

As to claim 2, Yamazaki et al. teaches a drive method for an EL display panel, the EL display panel comprising:

EL elements (fig. 3(111)) arranged in a matrix (fig. 2(101, 104));

driver transistors (fig. 3(109)) which supply current to be passed through the EL elements (fig. 3(111)); and

a gate driver circuit (fig. 1(103)) which selects pixel row of the EL display panel in sequence (col. 8, line 67 – col. 9, line 9).

Yamazaki et al. does not specifically teach an EL display panel where an operation for retaining an image signal applied to each pixel is retained only once during the one frame period.

Sekiya et al. teaches an EL display panel where an operation for retaining an image signal applied to each pixel is executed only once during the one frame period (col. 16, line 66 – col. 17, line 28).

Therefore, it is obvious to one skill in the art at the time of the invention was made to combine the image display panel apparatus of Sekiya et al. with the EL display device of Yamazaki et al. to make an EL display panel in order to improve quality of moving pictures.

Yamazaki et al. (as modified by Sekiya et al.) does not explicitly teach a start pulse to be input into the gate driver circuit is controlled, a plurality of stripe non-display areas on a EL display panel are generated, and the plurality of stripe non-display areas are moved in a scanning direction of the gate driver circuit.

Kamezaki et al. teaches a start pulse to be input into the gate driver circuit is controlled (col. 7, lines 38-45, col. 8, lines 21-28), a plurality of stripe non-display areas (fig. 2(1a)) on a EL display panel are generated, and the plurality of stripe non-display areas are moved in a scanning direction of the gate driver circuit (col. 4, lines 42-49, col. 7, lines 8-20).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to modify the drive method for an EL display of Yamazaki et al. (as modified by Sekiya et al.) using the idea of Kamezaki et al. of generating and moving a plurality of stripe non-display areas on a display screen in a scanning direction in order to achieve low power consumption and prevent flicker on a screen.

As to claim 4, Yamazaki et al. teaches a drive method for the EL display panel wherein the first switching elements (fig. 3(105)) are turned off periodically during one frame period (fig. 5).

As to claims 16 and 17, Yamazaki et al. discloses a drive method for the EL display panel wherein the driver transistors are P-channel transistors (col. 16, lines 6-9, as best understood).

As to claims 18 and 19, Sekiya et al. teaches an drive method for the EL display panel wherein brightness of the display screen is varied or controlled by varying proportion of the non-display area to a display area of the display screen (col. 4, lines 4-14, 42-49, col. 13, lines 60-67).

Response to Arguments

11. Applicant's arguments with respect to claims 1, 2, 4-7, 10, and 15-21 have been considered but are moot in view of the new ground(s) of rejection.

12. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AFROZA Y. CHOWDHURY whose telephone number is (571)270-1543. The examiner can normally be reached on 7:30-5:00 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC
9/22/2008
/Bipin Shalwala/
Supervisory Patent Examiner, Art Unit 2629